REMARKS

The Office Action dated March 18, 2004, has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

No new matter has been added, and no new issues are raised which require further consideration and/or search. Claims 23-52, 56, 57 and 58 have been allowed. Claims 1-15, 16,-22 and 53-55 are submitted for consideration.

As a preliminary matter, the Office Action indicated that claims 16 and 22 contain allowable subject matter, and would be allowable if amended to be in independent form. Applicant wishes to thank the Examiner for so indicating and Applicant addresses the independent claims, from which the allowable claims depend, below. Applicant also wishes to thank the Examiner for the allowance of claims 23-52, 56, 57 and 58.

Claims 1-7 and 53 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,424,565 to Larson in view of U.S. Patent No. 6,289,015 to Warner et al., further in view of U.S. Patent No. 6,381,247 to Munter et al. The rejection is traversed as being based on references that neither teach nor suggest the novel combination of features clearly recited in independent claims 1and 53. Claim 1, upon which claims 2-7 depend, recites a method of processing internal operations in a network switch. The method includes the step of constructing a lookup table in system memory, by snooping a communication channel in a network switch for lookup table information, and, upon detection of lookup table information on the communication channel,

transmitting the lookup table information to a remote system memory, thereby constructing a lookup table in the remote system memory. The method also includes the step of processing DMA operations by providing a DMA descriptor including a reload field therein, processing the DMA descriptor, and identifying a location of a next DMA descriptor based upon a condition of the reload field. The lookup table in remote system memory enables CPU access to the lookup table without requiring communication on the communication channel and the condition of the reload field enables flexible DMA descriptor handling.

Claim 53 recites a network switch for handling packets includes at least one lookup table therein. The lookup table is constructed based upon lookup messages transmitted over an internal communication channel and snoop logic connected to a remote system memory. The snoop logic also is connected to the internal communication channel to detect lookup table information being transmitted on the channel and transmit the lookup table information to the remote system memory. The snoop logic creates a duplicate lookup table in the remote system memory for direct memory access by a remote CPU. The network switch also includes a DMA unit containing DMA descriptor information therein. The DMA descriptor information includes a reload field and a DMA processing unit for processing the DMA descriptor information. The DMA processing unit identifies a location of a next DMA descriptor based upon a condition of the reload field. The DMA unit and the DMA processing unit enables efficient access to the remote system memory.

As will be discussed below, the cited prior art references of Larson, Warner et al. and Munter et al. fail to disclose or suggest the elements of any of the claims 1-7 and 53.

Larson teaches a high speed channel interface circuit between a communication channel and a processor and the processor memory. Col. 2, lines 40-44. The channel interface circuit monitors the communication channel to determine whether one of the data messages on the communication channel is destined for the processor memory, and if it is, the channel interface circuit stores the data message directly to the processor memory without requiring the involvement of the processor. Col. 2, lines 47-54. According to Larson, the reason for the channel interface circuit is to relieve the processor of the burden of supervising the receipt, decoding and storage of data messages transmitted on the communication channel to the processor memory. Col. 4, lines 64-68. The channel interface circuit accomplishes this function by receiving the data message, generating a hardware address based on the header field contained in the data message, using the hardware address to access a particular segment of memory in the processor memory and storing the data message therein. Col 4, line 68- Col. 5, line 6. The channel interface circuit contains three memory devices: an address matcher, a class encoder, and a DMA control table, each of which contains the tables that respectively provide header matching/selective listening, class identification and address generation functions. Col. 5, lines 52-60.

Specifically, the DMA control table functions as a hardware address generator responding to a class indication applied to its address leads by transmitting a 1 bit

address. Col. 9, lines 52-56. A state controller, which is a logic circuit which uses the clock signal from lead CLOCK and the feedback signal on leads STATE and MATCH to control the operation of various elements of the channel interface circuit, activates lead ENABLE either upon receipt of a match signal or upon completion of the data message and the receipt of an appropriate signal from an error checker on lead STATE, indicating the receipt of an error free message. Col. 9, lines 59-64. Thereafter, either the data message is stored as it is received or a transfer to the processor memory is performed only after the complete data message has been received. Col. 9, line 64 – Col. 10, line 2. If the message is stored as received, a DMA transfer unit directly stores the data message in the processor memory as soon as the header field is decoded by requesting access to the processor control, address and data busses, and when access is granted, by selecting the identified portion of the processor memory and storing the data message therein as it is being received. Col. 10, lines 2-15. Upon completion of the data transfer, the addresses in the DMA control table must be updated to reflect the new starting address for data storage based on the data message just stored in the processor memory. Col. 10, lines 15-24.

Warner et al. teaches a method for the secure switching of a packet within a communications network. Col. 2, lines 9-10. Warner et al. discloses a switch which includes ports, an array of MAC ports and an External Address Match (EAM) interface. Col. 4, lines 1-6. A DRAM memory resource is coupled to the switch core by a DRAM bus. An address-lookup device is coupled to the DRAM bus to actively snoop the

DRAM bus to implement the external address matching functionality of the switch. Col. 4, lines 47-57. Specifically, the address-lookup device captures both the source and destination addresses of a packet placed on the DRAM bus to generate the EAM signal and construct an address-lookup table. Col. 4, lines 57-61 and Col. 6, lines 32-35. The address-lookup table maps the source address of packets received at the switch to ports of the switch on which the respective packets were received. Col. 5, lines 2-5. The process of constructing the address-lookup table is referred to as the "learning" of addresses by the switch. Once an address/port record has been created in the address-lookup table, the switch is able to determine as to which port a packet having a "learned" destination address should be routed. Col. 5, lines 5-10.

Munter et al. teaches an implementation of a switch interface that is coupled between a fiber optic cable and a switching fabric. Col. 3, lines 8-11. The switch interface comprises a general processor and a local memory. Col. 3, lines 53-55 The local memory comprises program information and master look-up tables which may be kept at the individual memory devices in order to reduce the congestion on the general bus. Col. 13, lines 8-13.

Applicant submits that the combination of Larson, Warner et al. and Munter et al. fails to disclose or suggest the claimed features in each of claims 1-7 and 53. Claims 1 and 53 in part recites processing of DMA operations by providing a DMA descriptor including a reload field therein, processing the DMA descriptor, and identifying a location of a next DMA descriptor based upon a condition of the reload field. The Office

Action states that Fig. 7 and Col. 9 line 53 – Col. 10 line 23 of Larson teaches a DMA descriptor including a reload field and identifying a location of a next DMA descriptor based upon a condition of the reload field as recited in claims 1 and 53. As outline above, the DMA control table, as described in Larson, either stores a data message as it is received or transfers the message to the processor memory only after the complete data message has been received. Col. 9, line 64 – Col. 10, line 2. If the message is stored as received, Larson teaches that a DMA transfer unit directly stores the data message in the processor memory as soon as the header field is decoded by requesting access to the processor control, address and data busses, and when access is granted, by selecting the identified portion of the processor memory and storing the data message therein as it is being received. Col. 10, lines 2-15. Larson further teaches that upon completion of the data transfer, the addresses in the DMA control table must be updated to reflect the new starting address for data storage based on the data message just stored in the processor memory. Col. 10, lines 15-24. Applicant respectfully submits that Larson does not disclose or even suggest processing of DMA operations by providing a DMA descriptor including a reload field. In fact, there is simply no discussion in Larson of a DMA descriptor as recited in claims 1 and 53. Furthermore, there is no suggestion in Larson about processing the DMA descriptor and identifying a location of a next DMA descriptor based upon a condition of the reload field as recited in claims 1 and 53. Unlike claims 1 and 53, Larson does not suggest using the condition of a reload field to identify the location of a next DMA descriptor. Instead, Larson uses the data message just stored

in the processor memory to update the DMA look-up table and identify a new starting address for the next data message. Larson also does not disclose or suggest using the condition of the reload field to enable flexible DMA descriptor handling as recited in claim 1. Moreover, as stated in the Office Action Larson does not teach or suggest constructing a lookup table in system memory, by snooping a communication channel in a network switch for lookup table information, and, upon detection of lookup table information on the communication channel, transmitting the lookup table information to a remote system memory, thereby constructing a lookup table in the remote system memory as recited in claims 1 and 53. Additionally, Larson offers no suggestion or discussion of storing the look-up table in a remote system memory to enable CPU access to the look-up table without requiring communication on the communication channel as recited in claims 1 and 53.

Warner et al. does not cure any of the deficiencies of Larson with regard to claims 1 and 53 as outlined above. The Office Action states that Warner et al. discloses a process of constructing a look-up table by snooping the bus and that it is inherent in the purpose of snooping disclosed by Warner et al. that the look-up information will include insert message for newly found addresses and delete messages for addresses that are found to be no longer active. According to Warner et al., the address-look-up device snoops the bus for source and destination addresses and creates the address-look-up table to match the source and destination addresses to packets received on the switch. In claims 1 and 53, on the other hand, a lookup table is constructed in system memory by

snooping a communication channel in a network switch for lookup table information, and, upon detection of lookup table information on the communication channel, transmits the lookup table information to a remote system memory, thereby constructing a lookup table in the remote system memory. There is simply no discussion or suggestion in Warner et al. of constructing a look-up table in a remote system memory. Furthermore, like Larson, Warner et al. offers no suggestion or discussion of storing the look-up table in a remote system memory to enable CPU access to the look-up table without requiring communication on the communication channel as recited in claims 1 and 53.

The Office Action states that although Warner et al. and Larson do not teach transmitting the look-up table information to a remote memory, Munter et al. discloses that information may be kept in individual memory devices. In addition to not curing any of the deficiencies of Warner et al. and Larson as outlined above, Munter et al. simply does not suggest transmitting look-up table information to a remote memory to enable CPU access as recited by claims 1 and 53. The fact that Munter et al. teaches that look-up tables may be kept at individual memory devices in a processor to reduce congestion on a general bus does not suggest transmitting look-up table information to a remote memory to enable CPU access without requiring communication on the communication channel as recited by claims 1 and 53. Therefore, Applicant respectfully asserts that the rejection under 35 U.S.C. §103(a) should be withdrawn because neither Larson, Warner et al. nor Munter et al. whether taken singly or combined, teaches or suggests each feature of claims 1 and 53 and hence, dependent claim 2-7 thereon.

Claims 8-15 and 54 were rejected under 35 U.S.C. 103(a) as being unpatentable over Warner et al. in view of U.S. Patent No. 5,610,905 to Murthy et al. and further in view of Munter et al. The rejection is traversed as being based on references that neither teach nor suggest the novel combination of features clearly recited in independent claims 8 and 54. Claim 8 upon which claims 9-16 depend, recites a method of processing internal operations in a network switch. The method includes the steps of constructing a lookup table in system memory, by snooping a communication channel in a network switch for lookup table information, and, upon detection of address lookup table information on said communication channel, transmitting the lookup table information to a remote system memory, thereby constructing a lookup table in the remote system memory; monitoring port activity in the network switch, by storing port activity data in a statistics register on a network switch. The method also includes the steps of reading the port activity data with a statistics gathering unit; transmitting the port activity data directly to a remote system memory, thereby reconstructing the statistics register in the remote system memory, and then accessing the remote system memory with a remote CPU to read the reconstructed statistics register.

Claim 54 recites a network switch for handling packets. The network switch includes at least one lookup table therein. The lookup table is constructed based upon lookup messages transmitted over an internal communication channel. A snoop logic is connected to a remote system memory. The snoop logic also is connected to the internal communication channel to detect lookup table information being transmitted on said

channel and transmit the lookup table information to the remote system memory, wherein the snoop logic creates a duplicate lookup table in the remote system memory for direct memory access by a remote CPU. The network switch includes a data port for communicating with a data network. The network switch further includes a statistics counter connected to the data port for monitoring operational parameters associated with the data port, the statistics counter including statistics registers therein. The network switch also includes a statistics gathering circuit connected to the statistics counter for reading the statistics registers and for directly transmitting data from the statistics registers to the remote system memory.

As will be discussed below, the cited prior art references of Warner et al., Murthy et al. and Munter et al. fail to disclose or suggest the elements of claims 8-15 and 54.

Murthy et al. teaches a bridge to connect multiple packet-based segments of a network to allow efficient communications between stations on each network segment and also between stations located on different network segments connected to the bridge. Col. 4, lines 11-15. The bridge includes a monitoring device that is attached to a monitoring port. Col. 4, lines 51-52. According to Murthy et al., port monitoring is a process by which packets arriving at the bridge or generated internally may be copied to one or more monitoring ports. Col. 18, lines 22-24. The monitoring device attached to the monitoring port is able to provide analysis of monitored packets. The monitoring device analyzes packet traffic on the network and provides various diagnostic

information to enable the network manager to locate problems, evaluate performance and determine appropriate adjustments to network parameters. Col. 18, lines 24-34.

Applicant submits that the combination of Warner et al, Munter et al. and Murthy et al fails to disclose or suggest the claimed features of each of claims 8-15 and 54. The Office Action states that Warner et al. discloses a process of constructing a look-up table by snooping the bus and that it is inherent in the purpose of snooping disclosed by Warner et al. that the look-up information will include insert message for newly found addresses and delete messages for addresses that are found to be no longer active. According to Warner et al., the address-look-up device snoops the bus for source and destination addresses and creates the address-look-up table to match the source and destination addresses to packets received on the switch. In claims 8 and 54, on the other hand, a lookup table is constructed in system memory by snooping a communication channel in a network switch for lookup table information, and, upon detection of lookup table information on the communication channel, transmits the lookup table information to a remote system memory, thereby constructing a lookup table in the remote system memory. There is simply no discussion or suggestion in Warner et al. of constructing a look-up table in a remote system memory. Furthermore, Warner et al. offers no suggestion or discussion of storing the look-up table in a remote system memory to enable direct memory access by a remote CPU access as recited in claim 54. Additionally, as stated in the Office Action, Warner et al does not disclose or suggest

measuring port activity, sending those measurements to a remote memory and accessing the remote memory with a remote CPU to read the statistic register.

Murthy et al. does not cure any of the deficiencies of Warner et al. with regard to claims 8 and 54. Although the Office Action states that Murthy et al. teaches monitoring ports, Applicant submits that Murthy et al. teaches that port monitoring is a process by which packets arriving at the bridge or generated internally may be copied to one or more monitoring ports. Thereafter, according to Murthy et al., a monitoring device attached to the monitoring port is able to provide analysis of monitored packets by analyzing packet traffic on the network and providing various diagnostic information to enable the network manager to locate problems, evaluate performance and determine appropriate adjustments to network parameters. Murthy et al. simply does not teach or suggest monitoring port activity in a network switch by storing port activity in a statistics register on the switch, reading the port activity data with a statistic gathering unit, transmitting the port activity data directly to a remote system memory to reconstruct the statistic register in the remote system memory and accessing the remote system memory with a remote CPU to read the reconstructed statistic register as recited in claims 8 and 54.

The Office Action further states that although Warner et al. and Murthy et al. do not teach transmitting the look-up table information to a remote memory, Munter et al. discloses that information may be kept in individual memory devices. Applicant submits that Munter et al. does not cure any of the deficiencies of Warner et al. and Murthy et al as outlined above. Munter et al. does not teach or suggest transmitting look-up table

information to a remote memory to enable CPU access as recited by claims 8 and 54. As stated above, Munter et al. teaches that look-up tables may be kept at individual memory devices in a processor to reduce congestion on a general bus does which is different from transmitting look-up table information to a remote memory to enable remote CPU access as recited by claims 8 and 54. Therefore, Applicant respectfully asserts that the rejection under 35 U.S.C. §103(a) should be withdrawn because neither Warner et al., Murthy et al. nor Munter et al. whether taken singly or combined, teaches or suggests each feature of claims 8 and 54 and hence, dependent claim 9-15 thereon.

Claims 17-21 and 55 were rejected under 35 U.S.C. 103(a) as being unpatentable over Larson in view of Murthy et al. and further in view of Munter et al. The rejection is traversed as being based on references that neither teach nor suggest the novel combination of features clearly recited in independent claims 17 and 55. Claim 17, upon which claims 18-21 depend, recites a method of handling internal operations in a network switch. The method includes the steps of monitoring port activity in a network switch, by storing port activity data in a statistics register on the network switch and reading the port activity data with a statistics gathering unit. The method also includes the steps of transmitting the port activity data directly to a remote system memory, thereby reconstructing the statistics register in the remote system memory, and accessing the remote system memory with a remote CPU to read the reconstructed statistics register. The method further comprising the steps of processing DMA operations by performing the steps of providing a DMA descriptor, said DMA descriptor including a reload field

therein, processing said DMA descriptor, and identifying a location of a next DMA descriptor based upon a condition of the reload field.

Claim 55 recites a network switch including a data port for communicating with a data network. The network switch also includes a statistics counter connected to the data port for monitoring operational parameters associated with the data port, the statistics counter including statistics registers therein. The network switch further includes a statistics gathering circuit connected to the statistics counter for reading the statistics registers and for directly transmitting data from the statistics registers to a remote system memory. The network switch also includes a DMA unit containing DMA descriptor information therein. The DMA descriptor information includes a reload field. The network switch also includes DMA processing unit for processing the DMA descriptor information. The processing unit identifies a location of a next DMA descriptor based upon a condition of the reload field, wherein the DMA unit and the DMA processing unit work in conjunction with the remote system memory.

Applicant submits that the combination of Larson, Munter et al. and Murthy et al fails to disclose or suggest the claimed features of each of claims 17-21 and 55. Claims 17 and 55 in part recite processing of DMA operations by providing a DMA descriptor including a reload field therein, processing the DMA descriptor, and identifying a location of a next DMA descriptor based upon a condition of the reload field. The Office Action states that Fig. 7 and Col. 9 line 53 – Col. 10 line 23 of Larson teaches a DMA descriptor including a reload field and identifying a location of a next DMA descriptor

based upon a condition of the reload field as recited in claims 1 and 53. As outline above, Larson states that if the message is stored as received, a DMA transfer unit directly stores the data message in the processor memory as soon as the header field is decoded by requesting access to the processor control, address and data busses, and when access is granted, by selecting the identified portion of the processor memory and storing the data message therein as it is being received. Col. 10, lines 2-15. Larson further teaches that upon completion of the data transfer, the addresses in the DMA control table must be updated to reflect the new starting address for data storage based on the data message just stored in the processor memory. Col. 10, lines 15-24. Applicant respectfully submits that Larson does not disclose or even suggest processing of DMA operations by providing a DMA descriptor including a reload field. In fact, there is simply no discussion in Larson of a DMA descriptor as recited in claims 17 and 55. Furthermore, there is no suggestion in Larson about processing the DMA descriptor and identifying a location of a next DMA descriptor based upon a condition of the reload field as recited in claims 17 and 55. Larson also does not suggest using the condition of a reload field to identify the location of a next DMA descriptor as recited in claims 17 and 55. Instead, Larson uses the data message just stored in the processor memory to update the DMA look-up table and identify a new starting address for the next data message. Moreover, as stated in the Office Action Larson does not teach or suggest port monitoring wherein the monitoring information is sent to a remote memory location.

Murthy et al. does not cure any of the deficiencies of Larson with regard to claims 17 and 55. Although the Office Action states that Murthy et al. teaches monitoring ports, Applicant submits that Murthy et al. teaches that port monitoring is a process by which packets arriving at the bridge or generated internally may be copied to one or more monitoring ports. Thereafter, according to Murthy et al., a monitoring device attached to the monitoring port is able to provide analysis of monitored packets by analyzing packet traffic on the network and providing various diagnostic information to enable the network manager to locate problems, evaluate performance and determine appropriate adjustments to network parameters. Murthy et al. simply does not teach or suggest monitoring port activity in a network switch by storing port activity in a statistics register on the switch, reading the port activity data with a statistic gathering unit, transmitting the port activity data directly to a remote system memory to reconstruct the statistic register in the remote system memory and accessing the remote system memory with a remote CPU to read the reconstructed statistic register as recited in claims 17 and 55.

The Office Action states that although Murthy et al and Larson do not teach transmitting the look-up table information to a remote memory, Munter et al. discloses that information may be kept in individual memory devices. In addition to not curing any of the deficiencies of Murthy et al. and Larson as outlined above, Munter et al. simply does not suggest transmitting look-up table information to a remote memory to enable CPU access as recited by claims 1 and 53. The fact that Munter et al. teaches that look-up tables may be kept at individual memory devices in a processor to reduce congestion

on a general bus does not suggest transmitting look-up table information to a remote memory to enable CPU access without requiring communication on the communication channel as recited by claims 17 and 55. Therefore, Applicant respectfully asserts that the rejection under 35 U.S.C. §103(a) should be withdrawn because neither Larson, Warner et al. nor Munter et al. whether taken singly or combined, teaches or suggests each feature of claims 17 and 55 and hence, dependent claim 18-21 thereon.

Furthermore, Applicant respectfully submits that the Office Action has pieced together four references to teach the claimed invention. However, MPEP 2143.01 instructs that "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ 2d 1430 (Fed. Cir. 1990)." MPEP 2143.01 further instructs that "[a]lthough a prior art device 'may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so.'" Applicant respectfully submits that the cited references do not provide such a suggestion or motivation. Applicant submits that the only motivation to piece together the four references of the Office Action is found in Applicant's own invention. MPEP 2141, under the heading "Basic Consideration Which Apply to Obviousness Rejections," points out that "the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention." (See also Hodosh v. Block Drug Co., Inc. 786 F.2d 1136, 229 USPQ 182 (Fed. Cir. 1986).) The Federal Circuit has clearly held that "the motivation to combine references

cannot come from the invention itself." Heidelberger Druckmaschinen AG v. Hantscho Commercial Products, Inc., 21 F.3d 1068, 30 USPQ 2d 1377 (Fed. Cir. 1993).

In view of MPEP 2144.03, absent any teaching or suggestion in the prior art to adapt the teachings of Larson or Warner et al. to meet the claimed invention, and because the rejection lacks evidence of a teaching or suggestion that the features would have been obvious to one of ordinary skill, the rejections under 35 U.S.C. §103(a) are improper.

As noted previously, claims 1-22 and 53-55 recite subject matter which is neither disclosed nor suggested in the prior art references cited in the Office Action. It is therefore respectfully requested that all of claims 1-22 and 53-55 be allowed and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

Arlene P. Neal
Registration No. 43,828

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

APN:lls